ESP32-S3-WROOM-2

Datasheet

2.4 GHz Wi-Fi (802.11 b/g/n) and Bluetooth® 5 (LE) module
Built around ESP32-S3R8V SoC, Xtensa® dual-core 32-bit LX7 microprocessor
Flash up to 32 MB (Octal), 8 MB PSRAM (Octal)
33 GPIOs, rich set of peripherals
On-board PCB antenna

ESP32-S3-WROOM-2

Version 1.1
Espressif Systems

1 Module Overview

Note:

Check the link or the QR code to make sure that you use the latest version of this document:
https://www.espressif.com/documentation/esp32-s3-wroom-2_datasheet_en.pdf

1.1 Features

CPU and On-Chip Memory

- ESP32-S3R8V SoC embedded, Xtensa® dual-core 32-bit LX7 microprocessor (with single precision FPU), up to 240 MHz
- 384 KB ROM
- 512 KB SRAM
- 16 KB SRAM in RTC
- 8 MB PSRAM

Wi-Fi

- 802.11 b/g/n
- Bit rate: 802.11n up to 150 Mbps
- A-MPDU and A-MSDU aggregation
- 0.4 μs guard interval support
- Center frequency range of operating channel: 2412 ~ 2484 MHz

Bluetooth

- Bluetooth LE: Bluetooth 5, Bluetooth mesh
- Speed: 125 Kbps, 500 Kbps, 1 Mbps, 2 Mbps
- Advertising extensions
- Multiple advertisement sets
- Channel selection algorithm #2
- Internal co-existence mechanism between Wi-Fi and Bluetooth to share the same antenna

Peripherals

- GPIO, SPI, LCD interface, Camera interface, UART, I2C, I2S, remote control, pulse counter, LED PWM, USB 1.1 OTG, USB Serial/JTAG controller, MCPWM, SDIO host, GDMA, TWAI® controller (compatible with ISO 11898-1), ADC, touch sensor, temperature sensor, timers and watchdogs

Note:

* Please refer to *ESP32-S3 Series Datasheet* for detailed information about the module peripherals.

Integrated Components on Module

- 40 MHz crystal oscillator
- Up to 32 MB Octal SPI flash

Antenna Options

- On-board PCB antenna

Operating Conditions

- Operating voltage/Power supply: 3.0 ~ 3.6 V
- Operating ambient temperature: –40 ~ 65 °C

Certification

- RF certification: See certificates
- Green certification: RoHS/REACH

Test

- HTOL/HTSL/uHAST/TCT/ESD

1.2 Description

ESP32-S3-WROOM-2 is a powerful, generic Wi-Fi + Bluetooth LE MCU module that has a rich set of peripherals. It provides acceleration for neural network computing and signal processing workloads. It is an ideal choice for a wide variety of application scenarios related to AI and Artificial Intelligence of Things (AIoT), such as wake word detection and speech commands recognition, face detection and recognition, smart home, smart appliances, smart control panel, smart speaker, etc.

ESP32-S3-WROOM-2 comes with a PCB antenna. It has ESP32-S3R8V SoC embedded. A selection of module variants are available for customers with flash memory of 16/32 MB and PSRAM memory of 8 MB. Please note that for R8 series modules (8-line PSRAM embedded), if the PSRAM ECC function is enabled, the maximum ambient temperature can be improved to 85 °C, while the usable size of PSRAM will be reduced by 1/16.

The series comparison for ESP32-S3-WROOM-2 is as follows:

Table 1: ESP32-S3-WROOM-2 Series Comparison

Ordering Code	Flash	PSRAM[1]	Ambient Temp.[2] (°C)	Size[3] (mm)
ESP32-S3-WROOM-2-N16R8V	16 MB (Octal SPI)	8 MB (Octal SPI)	–40 ~ 65	18.0 × 25.5 × 3.1
ESP32-S3-WROOM-2-N32R8V	32 MB (Octal SPI)			

[1] This module uses PSRAM integrated in the chip's package.

[2] Ambient temperature specifies the recommended temperature range of the environment immediately outside the Espressif module.

[3] For details, refer to Section 7.1 *Physical Dimensions*.

At the core of the modules is an ESP32-S3R8V, an Xtensa® 32-bit LX7 CPU that operates at up to 240 MHz. You can power off the CPU and make use of the low-power co-processor to constantly monitor the peripherals for changes or crossing of thresholds.

ESP32-S3R8V integrates a rich set of peripherals including SPI, LCD interface, Camera interface, UART, I2C, I2S, remote control, pulse counter, LED PWM, USB Serial/JTAG controller, MCPWM, SDIO host, GDMA, TWAI® controller (compatible with ISO 11898-1), ADC, touch sensor, temperature sensor, timers and watchdogs, as well as up to 45 GPIOs. It also includes a full-speed USB 2.0 On-The-Go (OTG) interface to enable USB communication.

Note:

* For more information on ESP32-S3, please refer to *ESP32-S3 Series Datasheet*.

1.3 Applications

- Generic Low-power IoT Sensor Hub
- Generic Low-power IoT Data Loggers
- Cameras for Video Streaming
- Over-the-top (OTT) Devices
- USB Devices
- Speech Recognition
- Image Recognition
- Mesh Network
- Home Automation
- Smart Building

- Industrial Automation
- Smart Agriculture
- Audio Applications
- Health Care Applications
- Wi-Fi-enabled Toys
- Wearable Electronics
- Retail & Catering Applications

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2 Block Diagram

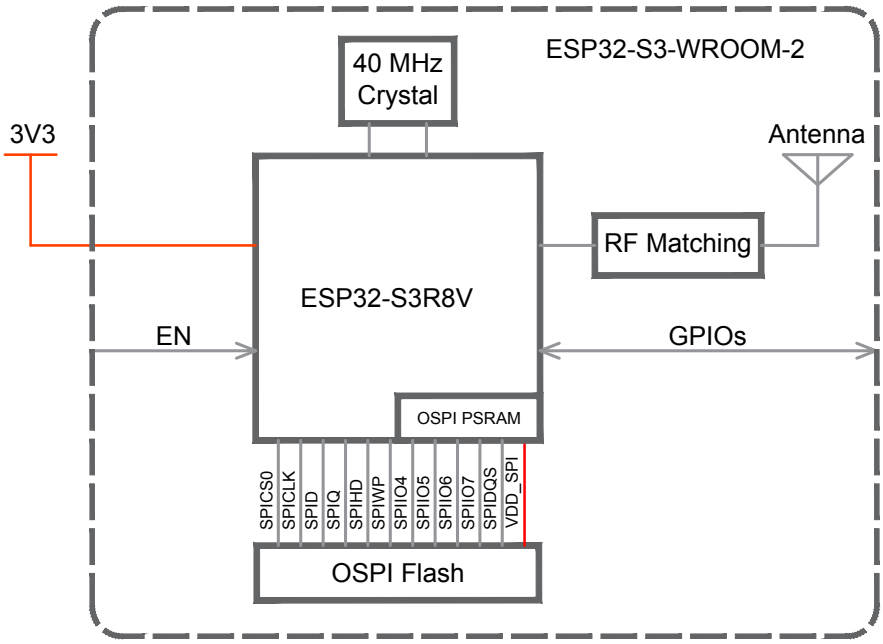

Figure 1: ESP32-S3-WROOM-2 Block Diagram

3 Pin Definitions

3.1 Pin Layout

The pin diagram below shows the approximate location of pins on the module. For the actual diagram drawn to scale, please refer to Figure 7.1 *Physical Dimensions*.

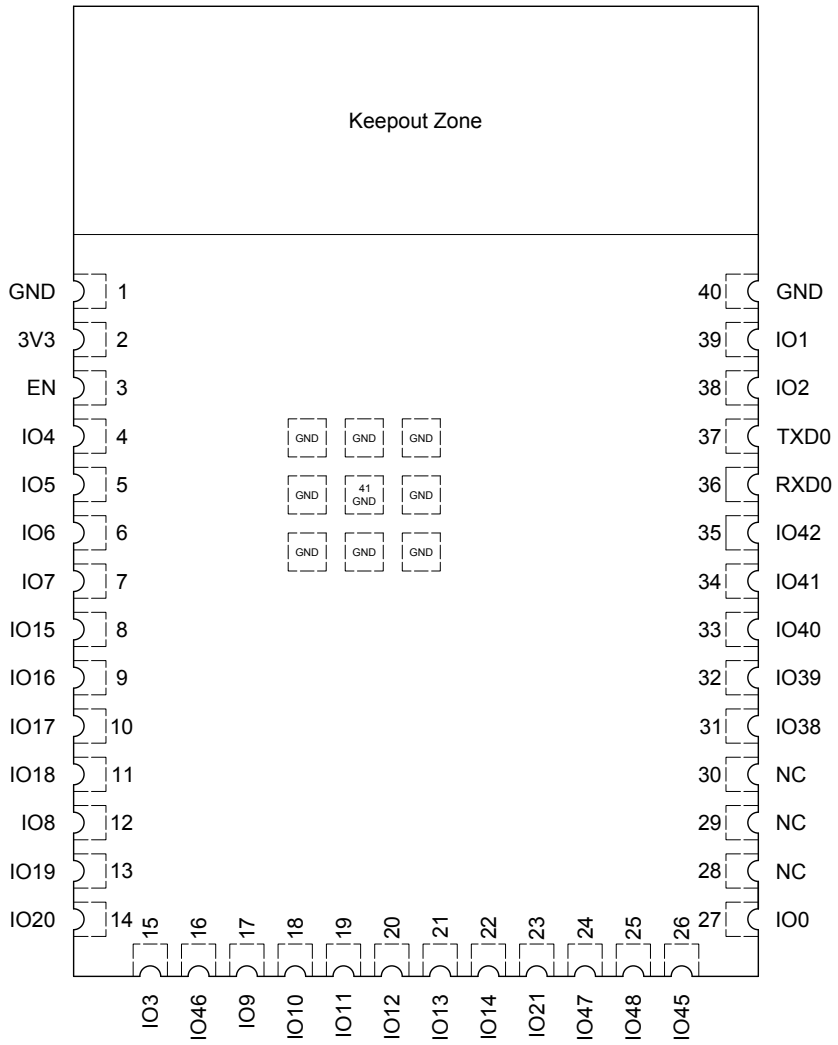

Figure 2: Pin Layout (Top View)

3.2 Pin Description

The module has 41 pins. See pin definitions in Table 2 *Pin Definitions*.

For explanations of pin names and function names, as well as configurations of peripheral pins, please refer to *ESP32-S3 Series Datasheet*.

Table 2: Pin Definitions

Name	No.	Type [1]	Function
GND	1	P	GND

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Table 2 – cont'd from previous page

Name	No.	Type [1]	Function
3V3	2	P	Power supply
EN	3	I	High: on, enables the chip. Low: off, the chip powers off. Note: Do not leave the EN pin floating.
IO4	4	I/O/T	RTC_GPIO4, **GPIO4**, TOUCH4, ADC1_CH3
IO5	5	I/O/T	RTC_GPIO5, **GPIO5**, TOUCH5, ADC1_CH4
IO6	6	I/O/T	RTC_GPIO6, **GPIO6**, TOUCH6, ADC1_CH5
IO7	7	I/O/T	RTC_GPIO7, **GPIO7**, TOUCH7, ADC1_CH6
IO15	8	I/O/T	RTC_GPIO15, **GPIO15**, U0RTS, ADC2_CH4, XTAL_32K_P
IO16	9	I/O/T	RTC_GPIO16, **GPIO16**, U0CTS, ADC2_CH5, XTAL_32K_N
IO17	10	I/O/T	RTC_GPIO17, **GPIO17**, U1TXD, ADC2_CH6
IO18	11	I/O/T	RTC_GPIO18, **GPIO18**, U1RXD, ADC2_CH7, CLK_OUT3
IO8	12	I/O/T	RTC_GPIO8, **GPIO8**, TOUCH8, ADC1_CH7, SUBSPICS1
IO19	13	I/O/T	RTC_GPIO19, GPIO19, U1RTS, ADC2_CH8, CLK_OUT2, **USB_D-**
IO20	14	I/O/T	RTC_GPIO20, GPIO20, U1CTS, ADC2_CH9, CLK_OUT1, **USB_D+**
IO3	15	I/O/T	RTC_GPIO3, **GPIO3**, TOUCH3, ADC1_CH2
IO46	16	I/O/T	**GPIO46**
IO9	17	I/O/T	RTC_GPIO9, **GPIO9**, TOUCH9, ADC1_CH8, FSPIHD, SUBSPIHD
IO10	18	I/O/T	RTC_GPIO10, **GPIO10**, TOUCH10, ADC1_CH9, FSPICS0, FSPIIO4, SUBSPICS0
IO11	19	I/O/T	RTC_GPIO11, **GPIO11**, TOUCH11, ADC2_CH0, FSPID, FSPIIO5, SUBSPID
IO12	20	I/O/T	RTC_GPIO12, **GPIO12**, TOUCH12, ADC2_CH1, FSPICLK, FSPIIO6, SUBSPICLK
IO13	21	I/O/T	RTC_GPIO13, **GPIO13**, TOUCH13, ADC2_CH2, FSPIQ, FSPIIO7, SUBSPIQ
IO14	22	I/O/T	RTC_GPIO14, **GPIO14**, TOUCH14, ADC2_CH3, FSPIWP, FSPIDQS, SUBSPIWP
IO21	23	I/O/T	RTC_GPIO21, **GPIO21**
IO47	24	I/O/T	SPICLK_P_DIFF, **GPIO47**[2], SUBSPICLK_P_DIFF
IO48	25	I/O/T	SPICLK_N_DIFF, **GPIO48**[2], SUBSPICLK_N_DIFF
IO45	26	I/O/T	**GPIO45**
IO0	27	I/O/T	RTC_GPIO0, **GPIO0**
NC	28	-	NC
NC	29	-	NC
NC	30	-	NC
IO38	31	I/O/T	**GPIO38**, FSPIWP, SUBSPIWP
IO39	32	I/O/T	**MTCK**, GPIO39, CLK_OUT3, SUBSPICS1
IO40	33	I/O/T	**MTDO**, GPIO40, CLK_OUT2
IO41	34	I/O/T	**MTDI**, GPIO41, CLK_OUT1
IO42	35	I/O/T	**MTMS**, GPIO42
RXD0	36	I/O/T	**U0RXD**, GPIO44, CLK_OUT2

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Table 2 – cont'd from previous page

Name	No.	Type [1]	Function
TXD0	37	I/O/T	**U0TXD**, GPIO43, CLK_OUT1
IO2	38	I/O/T	RTC_GPIO2, **GPIO2**, TOUCH2, ADC1_CH1
IO1	39	I/O/T	RTC_GPIO1, **GPIO1**, TOUCH1, ADC1_CH0
GND	40	P	GND
EPAD	41	P	GND

[1] P: power supply; I: input; O: output; T: high impedance. Bold font is the default function of the pin.

[2] As the VDD_SPI voltage of the ESP32-S3R8V chip has been set to 1.8 V, the working voltage for GPIO47 and GPIO48 would also be 1.8 V, which is different from other GPIOs.

3.3 Strapping Pins

Note:
The content below is excerpted from *ESP32-S3 Series Datasheet* > Section *Strapping Pins*. For the strapping pin mapping between the chip and modules, please refer to Chapter 5 *Module Schematics*.

At each startup or reset, a module requires some initial configuration parameters, such as in which boot mode to load the module, voltage of flash memory, etc. These parameters are passed over via the strapping pins. After reset, the strapping pins operate as regular IO pins.

The parameters controlled by the given strapping pins at module reset are as follows:

- **Chip boot mode** – GPIO0 and GPIO46
- **VDD_SPI voltage** – GPIO45
- **ROM messages printing** – GPIO46
- **JTAG signal source** – GPIO3

GPIO0, GPIO45, and GPIO46 are connected to the chip's internal weak pull-up/pull-down resistors at chip reset. These resistors determine the default bit values of the strapping pins. Also, these resistors determine the bit values if the strapping pins are connected to an external high-impedance circuit.

Table 3: Default Configuration of Strapping Pins

Strapping Pin	Default Configuration	Bit Value
GPIO0	Pull-up	1
GPIO3	Floating	–
GPIO45	Pull-down	0
GPIO46	Pull-down	0

To change the bit values, the strapping pins should be connected to external pull-down/pull-up resistances. If the ESP32-S3 is used as a device by a host MCU, the strapping pin voltage levels can also be controlled by the host MCU.

All strapping pins have latches. At system reset, the latches sample the bit values of their respective strapping pins and store them until the chip is powered down or shut down. The states of latches cannot be changed in any other way. It makes the strapping pin values available during the entire chip operation, and the pins are freed up to be used as regular IO pins after reset.

Regarding the timing requirements for the strapping pins, there are such parameters as *setup time* and *hold time*. For more information, see Table 4 and Figure 3.

Table 4: Description of Timing Parameters for the Strapping Pins

Parameter	Description	Min (ms)
t_{SU}	*Setup time* is the time reserved for the power rails to stabilize before the CHIP_PU pin is pulled high to activate the chip.	0
t_H	*Hold time* is the time reserved for the chip to read the strapping pin values after CHIP_PU is already high and before these pins start operating as regular IO pins.	3

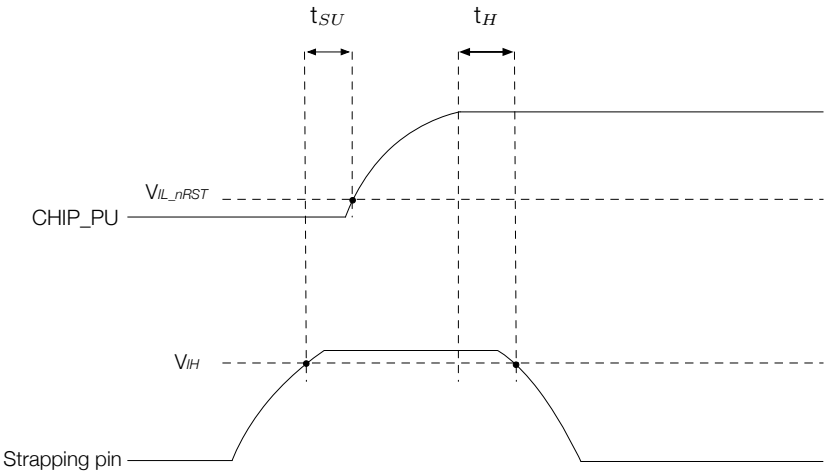

Figure 3: Visualization of Timing Parameters for the Strapping Pins

3.3.1 Chip Boot Mode Control

GPIO0 and GPIO46 control the boot mode after the reset is released. See Table 5 Chip Boot Mode Control.

Table 5: Chip Boot Mode Control

Boot Mode	GPIO0	GPIO46
Default Configuration	1 (Pull-up)	0 (Pull-down)
SPI Boot (default)	1	Any value
Download Boot	0	0
Invalid combination [1]	0	1

[1] This combination triggers unexpected behavior and should be avoided.

3.3.2 VDD_SPI Voltage Control

Depending on the value of EFUSE_VDD_SPI_FORCE, the voltage can be controlled in two ways.

Table 6: VDD_SPI Voltage Control

EFUSE_VDD_SPI_FORCE	GPIO45	eFuse [1]	Voltage	VDD_SPI power source [2]
0	0	Ignored	3.3 V	VDD3P3_RTC via R_{SPI}
	1		1.8 V	Flash Voltage Regulator
1	Ignored	0	1.8 V	Flash Voltage Regulator
		1	3.3 V	VDD3P3_RTC via R_{SPI}

[1] eFuse: EFUSE_VDD_SPI_TIEH

[2] See *ESP32-S3 Series Datasheet* > Section *Power Scheme*

3.3.3 ROM Messages Printing Control

During boot process the messages by the ROM code can be printed to:

- (Default) UART and USB Serial/JTAG controller.
- USB Serial/JTAG controller.
- UART.

The ROM messages printing to UART or USB Serial/JTAG controller can be respectively disabled by configuring registers and eFuse. For detailed information, please refer to *ESP32-S3 Technical Reference Manual* > Chapter *Chip Boot Control*.

3.3.4 JTAG Signal Source Control

The strapping pin GPIO3 can be used to control the source of JTAG signals during the early boot process. This pin does not have any internal pull resistors and the strapping value must be controlled by the external circuit that cannot be in a high impedance state.

As Table 7 shows, GPIO3 is used in combination with EFUSE_DIS_PAD_JTAG, EFUSE_DIS_USB_JTAG, and EFUSE_STRAP_JTAG_SEL.

Table 7: JTAG Signal Source Control

eFuse 1[a]	eFuse 2[b]	eFuse 3[c]	GPIO3	JTAG Signal Source
0	0	0	Ignored	USB Serial/JTAG Controller
		1	0	JTAG pins MTDI, MTCK, MTMS, and MTDO
			1	USB Serial/JTAG Controller
0	1	Ignored	Ignored	JTAG pins MTDI, MTCK, MTMS, and MTDO
1	0	Ignored	Ignored	USB Serial/JTAG Controller
1	1	Ignored	Ignored	JTAG is disabled

[a] eFuse 1: EFUSE_DIS_PAD_JTAG

[b] eFuse 2: EFUSE_DIS_USB_JTAG

[c] eFuse 3: EFUSE_STRAP_JTAG_SEL

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Stresses above those listed in Table 8 *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Table 9 *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 8: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
VDD33	Power supply voltage	–0.3	3.6	V
T_{STORE}	Storage temperature	–40	105	°C

4.2 Recommended Operating Conditions

Table 9: Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
VDD33	Power supply voltage	3.0	3.3	3.6	V
I_{VDD}	Current delivered by external power supply	0.5	—	—	A
T_A	Operating ambient temperature	–40	—	65	°C

4.3 DC Characteristics (3.3 V, 25 °C)

Table 10: DC Characteristics (3.3 V, 25 °C)

Symbol	Parameter	Min	Typ	Max	Unit
C_{IN}	Pin capacitance	—	2	—	pF
V_{IH}	High-level input voltage	0.75 × VDD[1]	—	VDD[1]+ 0.3	V
V_{IL}	Low-level input voltage	–0.3	—	0.25 × VDD[1]	V
I_{IH}	High-level input current	—	—	50	nA
I_{IL}	Low-level input current	—	—	50	nA
V_{OH}[2]	High-level output voltage	0.8 × VDD[1]	—	—	V
V_{OL}[2]	Low-level output voltage	—	—	0.1 × VDD[1]	V
I_{OH}	High-level source current (VDD[1]= 3.3 V, V_{OH} >= 2.64 V, PAD_DRIVER = 3)	—	40	—	mA
I_{OL}	Low-level sink current (VDD[1]= 3.3 V, V_{OL} = 0.495 V, PAD_DRIVER = 3)	—	28	—	mA
R_{PU}	Internal weak pull-up resistor	—	45	—	kΩ
R_{PD}	Internal weak pull-down resistor	—	45	—	kΩ
V_{IH_nRST}	Chip reset release voltage (EN voltage is within the specified range)	0.75 × VDD[1]	—	VDD[1]+ 0.3	V

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Table 10 – cont'd from previous page

Symbol	Parameter	Min	Typ	Max	Unit
V_{IL_nRST}	Chip reset voltage (EN voltage is within the specified range)	–0.3	—	0.25 × VDD[1]	V

[1] VDD is the I/O voltage for pins of a particular power domain.

[2] V_{OH} and V_{OL} are measured using high-impedance load.

4.4 Current Consumption Characteristics

4.4.1 RF Current Consumption in Active Mode

With the use of advanced power-management technologies, the module can switch between different power modes. For details on different power modes, please refer to Section *Low Power Management* in *ESP32-S3 Series Datasheet*.

Table 11: Current Consumption Depending on RF Modes

Work mode	Description		Peak (mA)
Active (RF working)	TX	802.11b, 1 Mbps, @20.5 dBm	355
		802.11g, 54 Mbps, @18 dBm	297
		802.11n, HT20, MCS 7, @17.5 dBm	286
		802.11n, HT40, MCS 7, @17 dBm	285
	RX	802.11b/g/n, HT20	95
		802.11n, HT40	97

[1] The current consumption measurements are taken with a 3.3 V supply at 25 °C of ambient temperature at the RF port. All transmitters' measurements are based on a 100% duty cycle.

[2] The current consumption figures for in RX mode are for cases when the peripherals are disabled and the CPU idle.

Note:
The content below is excerpted from *Section Power Consumption in Other Modes* in *ESP32-S3 Series Datasheet*.

4.4.2 Current Consumption in Other Modes

Please note that if the chip embedded has in-package PSRAM, the current consumption of the module might be higher compared to the measurements below.

Table 12: Current Consumption in Modem-sleep Mode

Work mode	Frequency (MHz)	Description	Typ[1] (mA)	Typ[2] (mA)
Modem-sleep[3]	40	WAITI (Dual core in idle state)	13.2	18.8
		Single core running 32-bit data access instructions, the other core in idle state	16.2	21.8
		Dual core running 32-bit data access instructions	18.7	24.4
		Single core running 128-bit data access instructions, the other core in idle state	19.9	25.4
		Dual core running 128-bit data access instructions	23.0	28.8
	80	WAITI	22.0	36.1
		Single core running 32-bit data access instructions, the other core in idle state	28.4	42.6
		Dual core running 32-bit data access instructions	33.1	47.3
		Single core running 128-bit data access instructions, the other core in idle state	35.1	49.6
		Dual core running 128-bit data access instructions	41.8	56.3
	160	WAITI	27.6	42.3
		Single core running 32-bit data access instructions, the other core in idle state	39.9	54.6
		Dual core running 32-bit data access instructions	49.6	64.1
		Single core running 128-bit data access instructions, the other core in idle state	54.4	69.2
		Dual core running 128-bit data access instructions	66.7	81.1
	240	WAITI	32.9	47.6
		Single core running 32-bit data access instructions, the other core in idle state	51.2	65.9
		Dual core running 32-bit data access instructions	66.2	81.3
		Single core running 128-bit data access instructions, the other core in idle state	72.4	87.9
		Dual core running 128-bit data access instructions	91.7	107.9

[1] Current consumption when all peripheral clocks are **disabled**.

[2] Current consumption when all peripheral clocks are **enabled**. In practice, the current consumption might be different depending on which peripherals are enabled.

[3] In Modem-sleep mode, Wi-Fi is clock gated, and the current consumption might be higher when accessing flash. For a flash rated at 80 Mbit/s, in SPI 2-line mode the consumption is 10 mA.

Table 13: Current Consumption in Low-Power Modes

Work mode	Description	Typ (μA)
Light-sleep[1]	VDD_SPI and Wi-Fi are powered down, and all GPIOs are high-impedance.	240
Deep-sleep	RTC memory and RTC peripherals are powered up.	8
	RTC memory is powered up. RTC peripherals are powered down.	7

Power off	CHIP_PU is set to low level. The chip is shut down.	1

[1] In Light-sleep mode, all related SPI pins are pulled up. For chips embedded with PSRAM, please add corresponding PSRAM consumption values, e.g., 140 μA for 8 MB 8-line PSRAM (3.3 V), 200 μA for 8 MB 8-line PSRAM (1.8 V) and 40 μA for 2 MB 4-line PSRAM (3.3 V).

4.5 Wi-Fi RF Characteristics

4.5.1 Wi-Fi RF Standards

Table 14: Wi-Fi RF Standards

Name		Description
Center frequency range of operating channel [1]		2412 ~ 2484 MHz
Wi-Fi wireless standard		IEEE 802.11b/g/n
Data rate	20 MHz	11b: 1, 2, 5.5 and 11 Mbps 11g: 6, 9, 12, 18, 24, 36, 48, 54 Mbps 11n: MCS0-7, 72.2 Mbps (Max)
	40 MHz	11n: MCS0-7, 150 Mbps (Max)
Antenna type		PCB antenna

[1] Device should operate in the center frequency range allocated by regional regulatory authorities. Target center frequency range is configurable by software.

4.5.2 Wi-Fi RF Transmitter (TX) Specifications

Target TX power is configurable based on device or certification requirements. The default characteristics are provided in Table 15 *TX Power with Spectral Mask and EVM Meeting 802.11 Standards*.

Table 15: TX Power with Spectral Mask and EVM Meeting 802.11 Standards

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11b, 1 Mbps	—	20.5	—
802.11b, 11 Mbps	—	20.5	—
802.11g, 6 Mbps	—	20.0	—
802.11g, 54 Mbps	—	18.0	—
802.11n, HT20, MCS 0	—	19.0	—
802.11n, HT20, MCS 7	—	17.5	—
802.11n, HT40, MCS 0	—	18.5	—
802.11n, HT40, MCS 7	—	17.0	—

Table 16: TX EVM Test

Rate	Min (dB)	Typ (dB)	SL[1] (dB)
802.11b, 1 Mbps, @20.5 dBm	—	–24.5	–10
802.11b, 11 Mbps, @20.5 dBm	—	–24.5	–10
802.11g, 6 Mbps, @20 dBm	—	–23.0	–5
802.11g, 54 Mbps, @18 dBm	—	–29.5	–25
802.11n, HT20, MCS 0, @19 dBm	—	–24.0	–5
802.11n, HT20, MCS 7, @17.5 dBm	—	–30.5	–27

Cont'd on next page

Table 16 – cont'd from previous page

Rate	Min (dB)	Typ (dB)	SL[1] (dB)
802.11n, HT40, MCS 0, @18.5 dBm	—	–25.0	–5
802.11n, HT40, MCS 7, @17 dBm	—	–30.0	–27

[1] SL stands for standard limit value.

4.5.3 Wi-Fi RF Receiver (RX) Specifications

Table 17: RX Sensitivity

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11b, 1 Mbps	—	–98.2	—
802.11b, 2 Mbps	—	–95.6	—
802.11b, 5.5 Mbps	—	–92.8	—
802.11b, 11 Mbps	—	–88.5	—
802.11g, 6 Mbps	—	–93.0	—
802.11g, 9 Mbps	—	–92.0	—
802.11g, 12 Mbps	—	–90.8	—
802.11g, 18 Mbps	—	–88.5	—
802.11g, 24 Mbps	—	–85.5	—
802.11g, 36 Mbps	—	–82.2	—
802.11g, 48 Mbps	—	–78.0	—
802.11g, 54 Mbps	—	–76.2	—
802.11n, HT20, MCS 0	—	–93.0	—
802.11n, HT20, MCS 1	—	–90.6	—
802.11n, HT20, MCS 2	—	–88.4	—
802.11n, HT20, MCS 3	—	–84.8	—
802.11n, HT20, MCS 4	—	–81.6	—
802.11n, HT20, MCS 5	—	–77.4	—
802.11n, HT20, MCS 6	—	–75.6	—
802.11n, HT20, MCS 7	—	–74.2	—
802.11n, HT40, MCS 0	—	–90.0	—
802.11n, HT40, MCS 1	—	–87.5	—
802.11n, HT40, MCS 2	—	–85.0	—
802.11n, HT40, MCS 3	—	–82.0	—
802.11n, HT40, MCS 4	—	–78.5	—
802.11n, HT40, MCS 5	—	–74.4	—
802.11n, HT40, MCS 6	—	–72.5	—
802.11n, HT40, MCS 7	—	–71.2	—

Table 18: Maximum RX Level

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11b, 1 Mbps	—	5	—
802.11b, 11 Mbps	—	5	—
802.11g, 6 Mbps	—	5	—
802.11g, 54 Mbps	—	0	—
802.11n, HT20, MCS 0	—	5	—
802.11n, HT20, MCS 7	—	0	—
802.11n, HT40, MCS 0	—	5	—
802.11n, HT40, MCS 7	—	0	—

Table 19: RX Adjacent Channel Rejection

Rate	Min (dB)	Typ (dB)	Max (dB)
802.11b, 1 Mbps	—	35	—
802.11b, 11 Mbps	—	35	—
802.11g, 6 Mbps	—	31	—
802.11g, 54 Mbps	—	14	—
802.11n, HT20, MCS 0	—	31	—
802.11n, HT20, MCS 7	—	13	—
802.11n, HT40, MCS 0	—	19	—
802.11n, HT40, MCS 7	—	8	—

4.6 Bluetooth LE Radio

Table 20: Bluetooth LE Frequency

Parameter	Min (MHz)	Typ (MHz)	Max (MHz)
Center frequency of operating channel	2402	—	2480

4.6.1 Bluetooth LE RF Transmitter (TX) Specifications

Table 21: Transmitter Characteristics - Bluetooth LE 1 Mbps

Parameter	Description	Min	Typ	Max	Unit
RF transmit power	RF power control range	–24.00	0	20.00	dBm
	Gain control step	—	3.00	—	dB
Carrier frequency offset and drift	Max $\lvert f_n \rvert_{n=0,\,1,\,2,\,..k}$	—	2.50	—	kHz
	Max $\lvert f_0 - f_n \rvert$	—	2.00	—	kHz
	Max $\lvert f_n - f_{n-5} \rvert$	—	1.40	—	kHz

Cont'd on next page

Table 21 – cont'd from previous page

Parameter	Description	Min	Typ	Max	Unit
	$\|f_1 - f_0\|$	—	1.00	—	kHz
Modulation characteristics	$\Delta\ f1_{avg}$	—	249.00	—	kHz
	Min $\Delta\ f2_{max}$ (for at least 99.9% of all $\Delta\ f2_{max}$)	—	198.00	—	kHz
	$\Delta\ f2_{avg}/\Delta\ f1_{avg}$	—	0.86	—	—
In-band spurious emissions	±2 MHz offset	—	–37.00	—	dBm
	±3 MHz offset	—	–42.00	—	dBm
	>±3 MHz offset	—	–44.00	—	dBm

Table 22: Transmitter Characteristics - Bluetooth LE 2 Mbps

Parameter	Description	Min	Typ	Max	Unit
RF transmit power	RF power control range	–24.00	0	20.00	dBm
	Gain control step	—	3.00	—	dB
Carrier frequency offset and drift	Max $\|f_n\|_{n=0,\ 1,\ 2,\ ..k}$	—	2.50	—	kHz
	Max $\|f_0 - f_n\|$	—	2.00	—	kHz
	Max $\|f_n - f_{n-5}\|$	—	1.40	—	kHz
	$\|f_1 - f_0\|$	—	1.00	—	kHz
Modulation characteristics	$\Delta\ f1_{avg}$	—	499.00	—	kHz
	Min $\Delta\ f2_{max}$ (for at least 99.9% of all $\Delta\ f2_{max}$)	—	416.00	—	kHz
	$\Delta\ f2_{avg}/\Delta\ f1_{avg}$	—	0.89	—	—
In-band spurious emissions	±4 MHz offset	—	–42.00	—	dBm
	±5 MHz offset	—	–44.00	—	dBm
	>±5 MHz offset	—	–47.00	—	dBm

Table 23: Transmitter Characteristics - Bluetooth LE 125 Kbps

Parameter	Description	Min	Typ	Max	Unit
RF transmit power	RF power control range	–24.00	0	20.00	dBm
	Gain control step	—	3.00	—	dB
Carrier frequency offset and drift	Max $\|f_n\|_{n=0,\ 1,\ 2,\ ..k}$	—	0.80	—	kHz
	Max $\|f_0 - f_n\|$	—	1.00	—	kHz
	$\|f_n - f_{n-3}\|$	—	0.30	—	kHz
	$\|f_0 - f_3\|$	—	1.00	—	kHz
Modulation characteristics	$\Delta\ f1_{avg}$	—	248.00	—	kHz
	Min $\Delta\ f1_{max}$ (for at least 99.9% of all$\Delta\ f1_{max}$)	—	222.00	—	kHz
In-band spurious emissions	±2 MHz offset	—	–37.00	—	dBm
	±3 MHz offset	—	–42.00	—	dBm
	>±3 MHz offset	—	–44.00	—	dBm

Table 24: Transmitter Characteristics - Bluetooth LE 500 Kbps

Parameter	Description	Min	Typ	Max	Unit
RF transmit power	RF power control range	–24.00	0	20.00	dBm
	Gain control step	—	3.00	—	dB
Carrier frequency offset and drift	Max $\|f_n\|_{n=0,\ 1,\ 2,\ ..k}$	—	0.80	—	kHz
	Max $\|f_0 - f_n\|$	—	1.00	—	kHz
	$\|f_n - f_{n-3}\|$	—	0.85	—	kHz
	$\|f_0 - f_3\|$	—	0.34	—	kHz
Modulation characteristics	$\Delta\ f2_{avg}$	—	213.00	—	kHz
	Min $\Delta\ f2_{max}$ (for at least 99.9% of all $\Delta\ f2_{max}$)	—	196.00	—	kHz
In-band spurious emissions	±2 MHz offset	—	–37.00	—	dBm
	±3 MHz offset	—	–42.00	—	dBm
	>±3 MHz offset	—	–44.00	—	dBm

4.6.2 Bluetooth LE RF Receiver (RX) Specifications

Table 25: Receiver Characteristics - Bluetooth LE 1 Mbps

Parameter	Description	Min	Typ	Max	Unit
Sensitivity @30.8% PER	—	—	–96.5	—	dBm
Maximum received signal @30.8% PER	—	—	8	—	dBm
Co-channel C/I	F = F0 MHz	—	9	—	dB
Adjacent channel selectivity C/I	F = F0 + 1 MHz	—	–3	—	dB
	F = F0 – 1 MHz	—	–3	—	dB
	F = F0 + 2 MHz	—	–28	—	dB
	F = F0 – 2 MHz	—	–30	—	dB
	F = F0 + 3 MHz	—	–31	—	dB
	F = F0 – 3 MHz	—	–33	—	dB
	F > F0 + 3 MHz	—	–32	—	dB
	F > F0 – 3 MHz	—	–36	—	dB
Image frequency	—	—	–32	—	dB
Adjacent channel to image frequency	F = F_{image} + 1 MHz	—	–39	—	dB
	F = F_{image} – 1 MHz	—	–31	—	dB
Out-of-band blocking performance	30 MHz ~ 2000 MHz	—	–9	—	dBm
	2003 MHz ~ 2399 MHz	—	–18	—	dBm
	2484 MHz ~ 2997 MHz	—	–15	—	dBm
	3000 MHz ~ 12.75 GHz	—	–5	—	dBm
Intermodulation	—	—	–29	—	dBm

Table 26: Receiver Characteristics - Bluetooth LE 2 Mbps

Parameter	Description	Min	Typ	Max	Unit
Sensitivity @30.8% PER	—	—	–92.5	—	dBm
Maximum received signal @30.8% PER	—	—	3	—	dBm
Co-channel C/I	F = F0 MHz	—	10	—	dB
Adjacent channel selectivity C/I	F = F0 + 2 MHz	—	–8	—	dB
	F = F0 – 2 MHz	—	–5	—	dB
	F = F0 + 4 MHz	—	–31	—	dB
	F = F0 – 4 MHz	—	–33	—	dB
	F = F0 + 6 MHz	—	–37	—	dB
	F = F0 – 6 MHz	—	–37	—	dB
	F > F0 + 6 MHz	—	–40	—	dB
	F > F0 – 6 MHz	—	–40	—	dB
Image frequency	—	—	–31	—	dB
Adjacent channel to image frequency	F = F_{image} + 2 MHz	—	–37	—	dB
	F = F_{image} – 2 MHz	—	–8	—	dB
Out-of-band blocking performance	30 MHz ~ 2000 MHz	—	–15	—	dBm
	2003 MHz ~ 2399 MHz	—	–19	—	dBm
	2484 MHz ~ 2997 MHz	—	–15	—	dBm
	3000 MHz ~ 12.75 GHz	—	–6	—	dBm
Intermodulation	—	—	–29	—	dBm

Table 27: Receiver Characteristics - Bluetooth LE 125 Kbps

Parameter	Description	Min	Typ	Max	Unit
Sensitivity @30.8% PER	—	—	–103.5	—	dBm
Maximum received signal @30.8% PER	—	—	8	—	dBm
Co-channel C/I	F = F0 MHz	—	6	—	dB
Adjacent channel selectivity C/I	F = F0 + 1 MHz	—	–6	—	dB
	F = F0 – 1 MHz	—	–5	—	dB
	F = F0 + 2 MHz	—	–32	—	dB
	F = F0 – 2 MHz	—	–39	—	dB
	F = F0 + 3 MHz	—	–35	—	dB
	F = F0 – 3 MHz	—	–45	—	dB
	F > F0 + 3 MHz	—	–35	—	dB
	F > F0 – 3 MHz	—	–48	—	dB
Image frequency	—	—	–35	—	dB
Adjacent channel to image frequency	F = F_{image} + 1 MHz	—	–49	—	dB
	F = F_{image} – 1 MHz	—	–32	—	dB

Table 28: Receiver Characteristics - Bluetooth LE 500 Kbps

Parameter	Description	Min	Typ	Max	Unit
Sensitivity @30.8% PER	—	—	–100	—	dBm
Maximum received signal @30.8% PER	—	—	8	—	dBm
Co-channel C/I	F = F0 MHz	—	4	—	dB
Adjacent channel selectivity C/I	F = F0 + 1 MHz	—	–5	—	dB
	F = F0 – 1 MHz	—	–5	—	dB
	F = F0 + 2 MHz	—	–28	—	dB
	F = F0 – 2 MHz	—	–36	—	dB
	F = F0 + 3 MHz	—	–36	—	dB
	F = F0 – 3 MHz	—	–38	—	dB
	F > F0 + 3 MHz	—	–37	—	dB
	F > F0 – 3 MHz	—	–41	—	dB
Image frequency	—	—	–37	—	dB
Adjacent channel to image frequency	F = F_{image} + 1 MHz	—	–44	—	dB
	F = F_{image} – 1 MHz	—	–28	—	dB

5 Module Schematics

This is the reference design of the module.

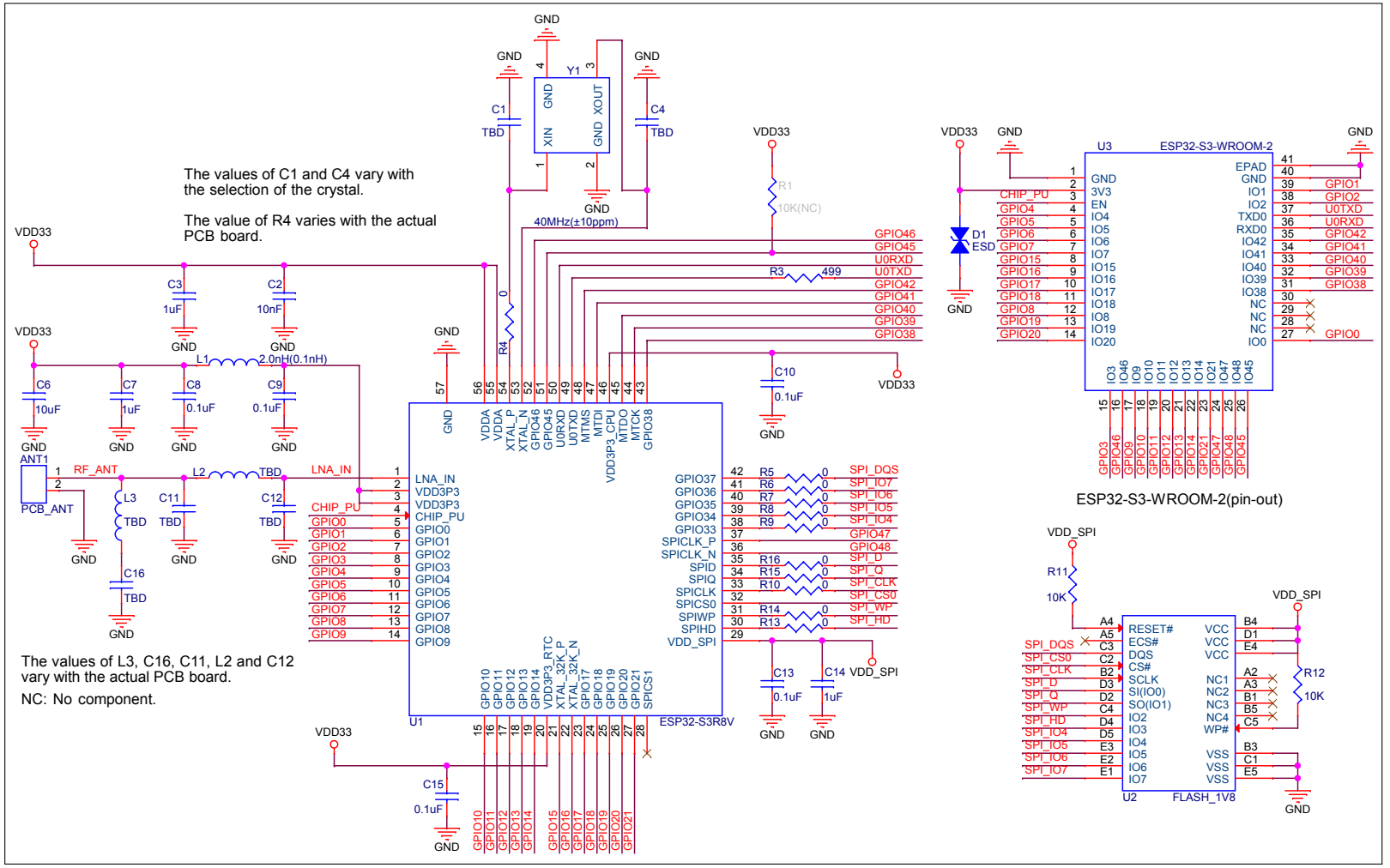


Figure 4: ESP32-S3-WROOM-2 Schematics

Note that for ESP32_S3R8V, VDD_SPI has been set to 1.8 V by eFuse VDD_SPI_TIEH and VDD_SPI_FORCE.

6 Peripheral Schematics

This is the typical application circuit of the module connected with peripheral components (for example, power supply, antenna, reset button, JTAG interface, and UART interface).

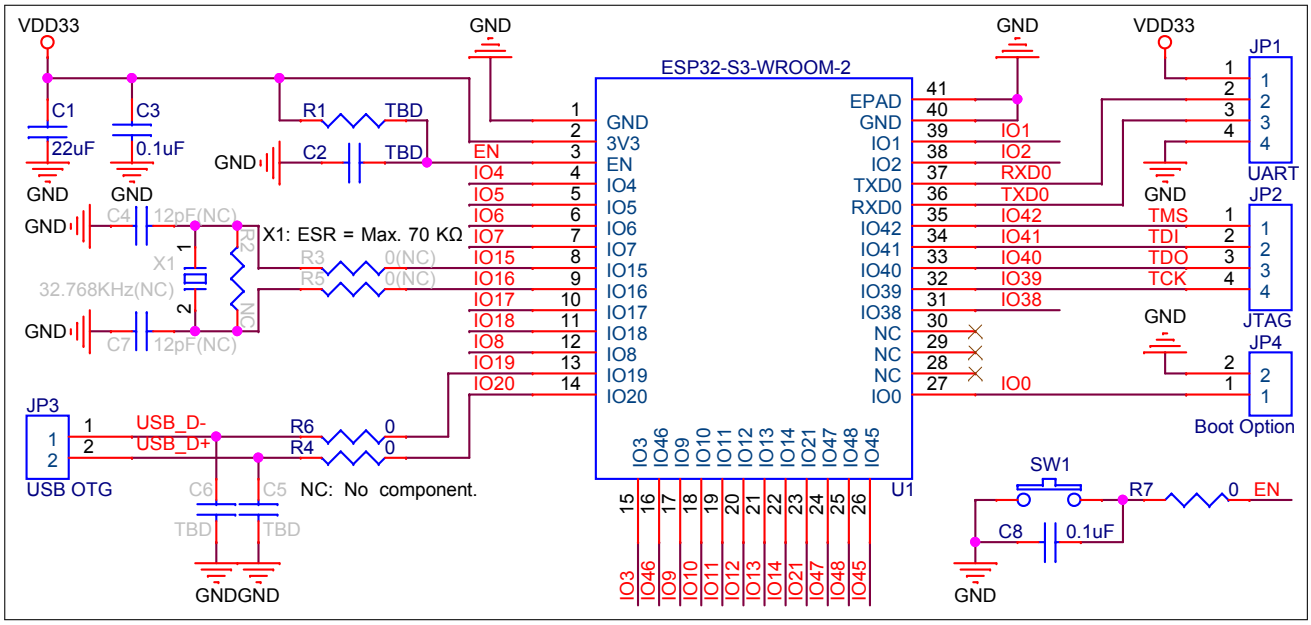


Figure 5: Peripheral Schematics

- Soldering the EPAD to the ground of the base board is not a must, however, it can optimize thermal performance. If you choose to solder it, please apply the correct amount of soldering paste. Too much soldering paste may increase the gap between the module and the baseboard. As result, the adhesion between other pins and the baseboard may be poor.
- To ensure that the power supply to the ESP32-S3 chip is stable during power-up, it is advised to add an RC delay circuit at the EN pin. The recommended setting for the RC delay circuit is usually R = 10 kΩ and C = 1 μF. However, specific parameters should be adjusted based on the power-up timing of the module and the power-up and reset sequence timing of the chip. For ESP32-S3's power-up and reset sequence timing diagram, please refer to *ESP32-S3 Series Datasheet* > Section *Power Supply*.

7 Physical Dimensions and PCB Land Pattern

7.1 Physical Dimensions

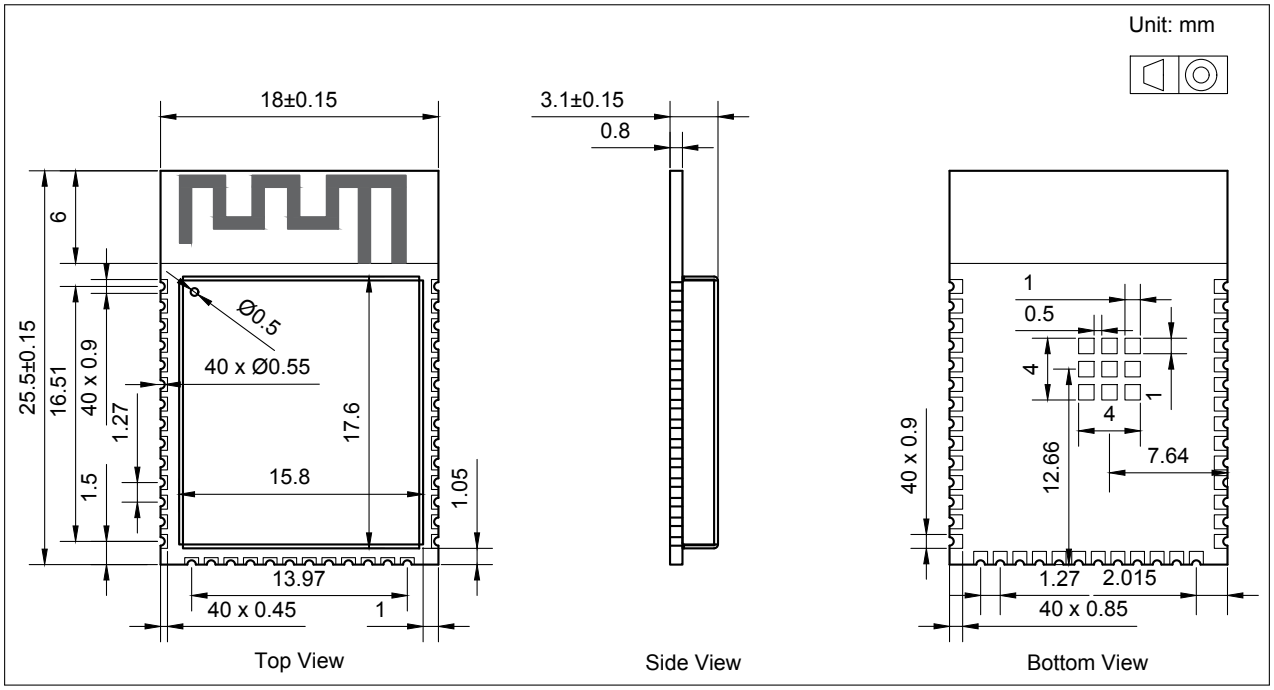


Figure 6: ESP32-S3-WROOM-2 Physical Dimensions

Note:
For information about tape, reel, and product marking, please refer to Espressif Module Packaging Information.

7.2 Recommended PCB Land Pattern

This section provides the following resources for your reference:

- Figure for recommended PCB land pattern with all the dimensions needed for PCB design. See Figure 7 *ESP32-S3-WROOM-2 Recommended PCB Land Pattern*.
- Source file of recommended PCB land pattern to measure dimensions not covered in Figure 7. You can view the source files for ESP32-S3-WROOM-2 with Autodesk Viewer.

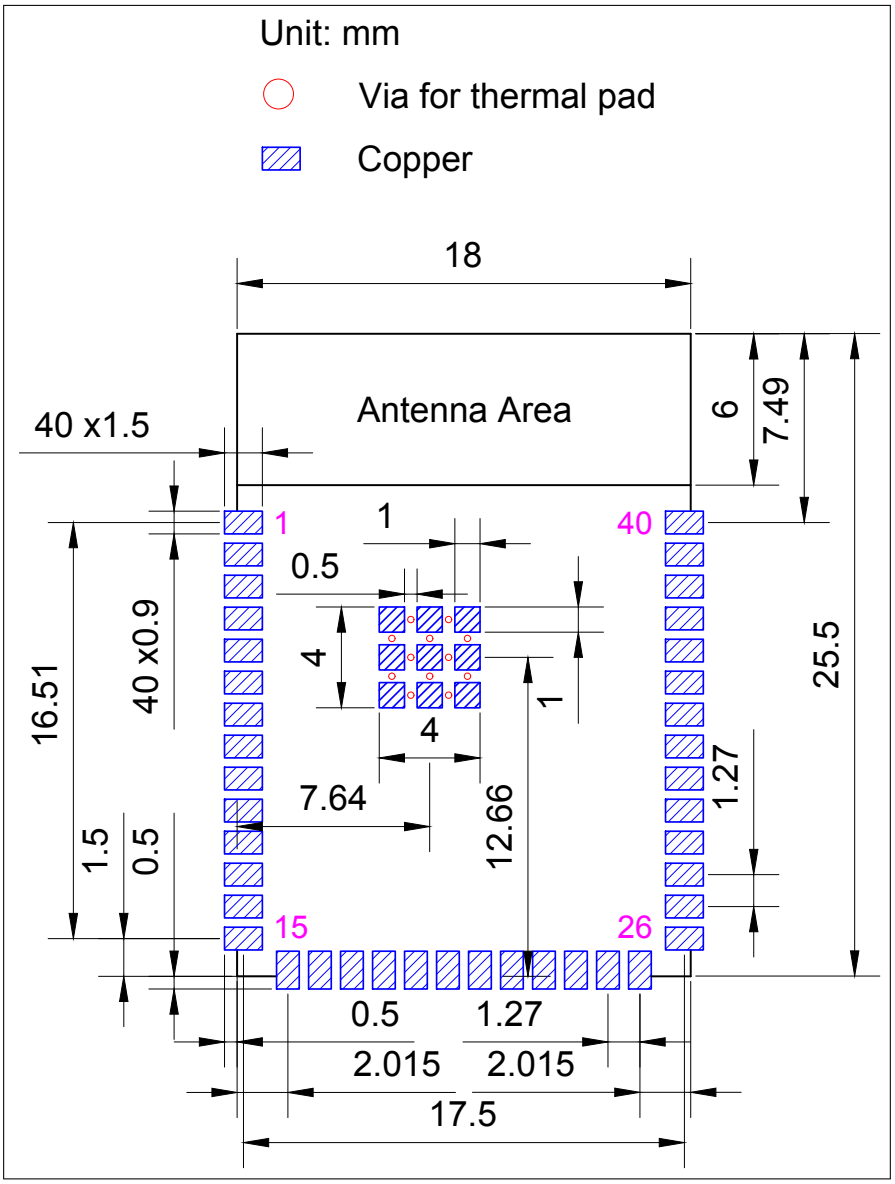


Figure 7: ESP32-S3-WROOM-2 Recommended PCB Land Pattern

8 Product Handling

8.1 Storage Conditions

The products sealed in moisture barrier bags (MBB) should be stored in a non-condensing atmospheric environment of < 40 °C and 90%RH. The module is rated at the moisture sensitivity level (MSL) of 3.

After unpacking, the module must be soldered within 168 hours with the factory conditions 25±5 °C and 60%RH. If the above conditions are not met, the module needs to be baked.

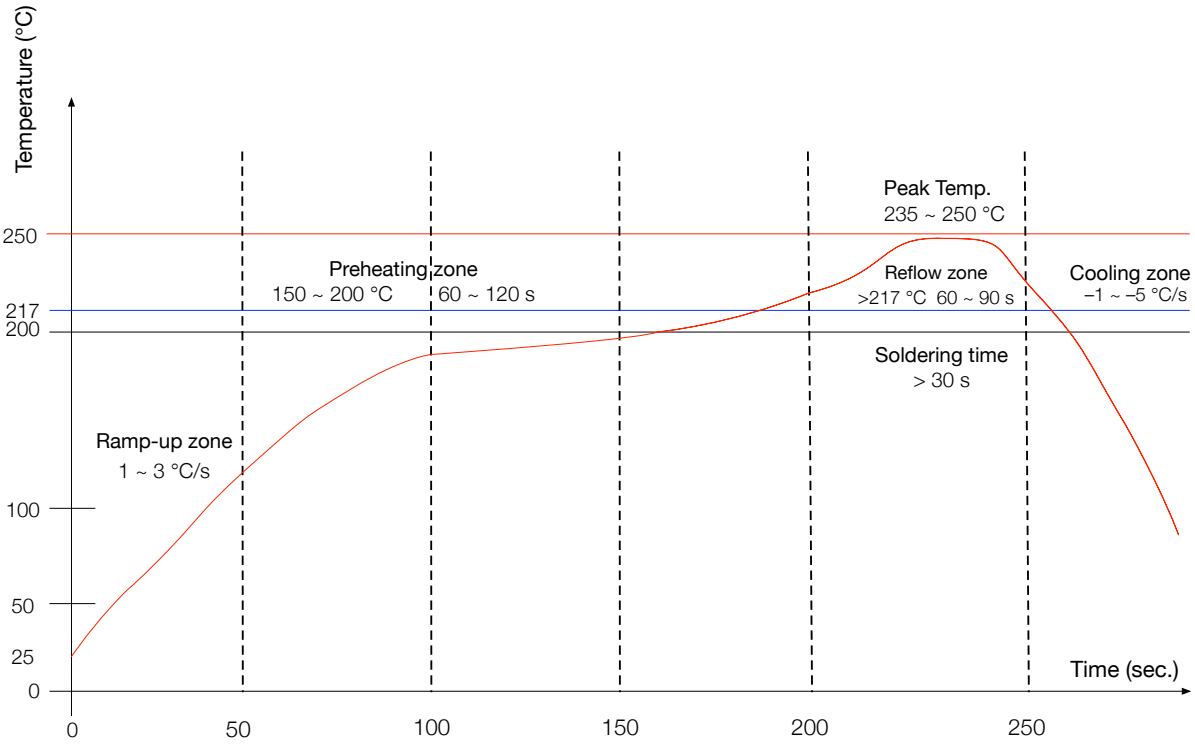
8.2 Electrostatic Discharge (ESD)

- Human body model (HBM): ±2000 V
- Charged-device model (CDM): ±500 V

8.3 Soldering Profile

8.3.1 Reflow Profile

Solder the module in a single reflow.



Ramp-up zone — Temp.: 25 ~ 150 °C Time: 60 ~ 90 s Ramp-up rate: 1 ~ 3 °C/s
Preheating zone — Temp.: 150 ~ 200 °C Time: 60 ~ 120 s
Reflow zone — Temp.: >217 °C Time: 60 ~ 90 s; Peak Temp.: 235 ~ 250 °C Time: 30 ~ 70 s
Cooling zone — Peak Temp. ~ 180 °C Ramp-down rate: –1 ~ –5 °C/s
Solder — Sn-Ag-Cu (SAC305) lead-free solder alloy

Figure 8: Reflow Profile

8.4 Ultrasonic Vibration

Avoid exposing Espressif modules to vibration from ultrasonic equipment, such as ultrasonic welders or ultrasonic cleaners. This vibration may induce resonance in the in-module crystal and lead to its malfunction or even failure. As a consequence, **the module may stop working or its performance may deteriorate**.

9 Related Documentation and Resources

Related Documentation

- ESP32-S3 Series Datasheet – Specifications of the ESP32-S3 hardware.
- ESP32-S3 Technical Reference Manual – Detailed information on how to use the ESP32-S3 memory and peripherals.
- ESP32-S3 Hardware Design Guidelines – Guidelines on how to integrate the ESP32-S3 into your hardware product.
- ESP32-S3 Series SoC Errata – Descriptions of known errors in ESP32-S3 series of SoCs.
- *Certificates*
  https://espressif.com/en/support/documents/certificates
- *ESP32-S3 Product/Process Change Notifications (PCN)*
  https://espressif.com/en/support/documents/pcns?keys=ESP32-S3
- *ESP32-S3 Advisories* – Information on security, bugs, compatibility, component reliability.
  https://espressif.com/en/support/documents/advisories?keys=ESP32-S3
- *Documentation Updates and Update Notification Subscription*
  https://espressif.com/en/support/download/documents

Developer Zone

- ESP-IDF Programming Guide for ESP32-S3 – Extensive documentation for the ESP-IDF development framework.
- *ESP-IDF* and other development frameworks on GitHub.
  https://github.com/espressif
- *ESP32 BBS Forum* – Engineer-to-Engineer (E2E) Community for Espressif products where you can post questions, share knowledge, explore ideas, and help solve problems with fellow engineers.
  https://esp32.com/
- *The ESP Journal* – Best Practices, Articles, and Notes from Espressif folks.
  https://blog.espressif.com/
- See the tabs *SDKs and Demos*, *Apps*, *Tools*, *AT Firmware*.
  https://espressif.com/en/support/download/sdks-demos

Products

- *ESP32-S3 Series SoCs* – Browse through all ESP32-S3 SoCs.
  https://espressif.com/en/products/socs?id=ESP32-S3
- *ESP32-S3 Series Modules* – Browse through all ESP32-S3-based modules.
  https://espressif.com/en/products/modules?id=ESP32-S3
- *ESP32-S3 Series DevKits* – Browse through all ESP32-S3-based devkits.
  https://espressif.com/en/products/devkits?id=ESP32-S3
- *ESP Product Selector* – Find an Espressif hardware product suitable for your needs by comparing or applying filters.
  https://products.espressif.com/#/product-selector?language=en

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Revision History

Date	Version	Release notes
2023-03-07	v1.1	• Update Section 3.3 *Strapping Pins* • Update Section 4.4 *Current Consumption Characteristics* • Update the Bluetooth maximum transmit power from 21 dBm to 20 dBm • Update descriptions in Section 6 *Peripheral Schematics* • Add descriptions in Section 7.2 *Recommended PCB Land Pattern* • Update Section 9 *Related Documentation and Resources* • Other minor changes
2022-11-01	v1.0	• Add certification and test information • Update Table 1 and Table 13 and add note • Update note in Table 2 • Update BLE RF power control range in Table 21 • Other minor updates
2022-05-09	v0.7	Update pin definitions table
2021-12-31	v0.6	Overall update for chip revision 1
2021-07-13	v0.1	Preliminary release, for chip revision 0

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